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(54) **Method of digital signal recording.**

(57) In the first method, a specific section provided in a track is set in DC free state, and when reproducing, accurate tracking is conducted on the basis of the crosstalk from the pilot tone superposed in the adjacent tracks in this DC free section. In the second method, a pilot tone is generated only in a specific section provided in the track, and when reproducing, accurate tracking is conducted on the basis of the crosstalk of the pilot tone in the tracks adjacent to this section. As a result, the quantity of redundancy required for tracking is notably reduced.

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The present Invention relates to a method of a digital signal recording suited to reproduction of recorded signals with few errors by accurately tracing the recording tracks formed on a recording medium.

When recording a digital signal magnetically in a narrow track, presently, in order to track accurately and reproduce the signals with fewest errors, pilot tones of several different frequencies are superposed in each track of the data to be recorded at the time of recording. For example, as shown in Fig. 2, using pilot tones of four different frequencies, a case of recording on a magnetic tape is explained below. In this case, the recording tracks continuously formed on the recording medium (hereinafter called tracks) are sequentially supposed to be T1, T2, T3, T4, and so forth. Besides, the frequency of the pilot tone to be superposed on track T1 is supposed to be f1 (Hz), the frequency of the pilot tone to be superposed on track T2 to be f2 (Hz), the frequency of the pilot tone to be superposed on track T3 to be f3 (Hz), and the frequency of the pilot tone to be superposed on track T4 to be f4 (Hz). The pilot tone frequencies f1 to f4 are recycled in a period of four tracks, and superposed on each track.

When reproducing, for example relating to track T2, by sampling and comparing the crosstalk levels of the pilot tones (fr Hz, f3 Hz) from the both side tracks T1, T3, the tracking is controlled so that the both levels be identical. In other words, it is controlled so that the center of the reproducing head when tracing the track T2 may correctly trace the center of the track T2. Then, by sampling and comparing the crosstalk levels of the both side pilot tones (f_2 Hz, f_4 Hz) while scanning the track T3, the tracking is controlled so that the both levels be identical. Similarly, while scanning the track T4, the crosstalk levels of the pilot tones (f_3 Hz, f_1 Hz) are compared to control. While scanning the track T5, the crosstalk levels of the pilot tones (f_4 Hz, f_2 Hz) are sampled and compared-to control the tracking. The crosstalk of each pilot tone is extracted by a band-pass filter from a reproduced signal.

In such constitution, in order to track accurately, the crosstalk level of the pilot tone of such an extent as not to be easily affected by noise must be detected by the bandpass filter to compare the levels. Or, for the pilot tone to be detected, the data components of the pertinent frequency may be also regarded as noise. Therefore, the recording level of the pilot tone must be higher than the level of the data signal by about more than ten or more than twenty decibels. However, when a pilot tone of such high level is superposed on the data signal analogously, it is equivalent to noise as seen from the data signal, and errors increase in the reproduced data. Or, to avoid this, when a pilot tone of high level is digitally added to the data signal, generally, the recording rate increases, thereby making it difficult to record and reproduce.

It is hence a primary object of the invention to present, in the light of the above background; a method of a digital signal recording capable of lowering the signal level of the pilot tone to be superposed, and a method of a digital signal recording low in the rate of increase of recording rate and capable of raising the level of the pilot tone to be superposed.

It is a first feature of the invention to set a signal in a specific section in a track to be a DC free state, out of signals recorded on a track. The frequency of the pilot tone is set at a relatively low frequency. Therefore, even in the case of azimuth recording, such low frequency component induces a relatively large crosstalk in an adjacent track. On the other hand, since the signal in the specific section in the track is in DC free state, the signal level near the pilot frequency in this section is sufficiently smaller than the crosstalk level of the pilot tones from the adjacent tracks. Thus, in the invention, since the DC component of the signal and spectrum of low frequency are lowered in a specific section, if the signal level of the pilot tone to be superposed is low, a necessary crosstalk level is obtained.

It is a second feature of the invention to set the frequency spectrum of the pilot tone of a signal in a specific section larger than the spectrum at the same frequency of a signal to be recorded outside this specific section, by adding redundant information only to the specific section in the track, of signals to be recorded in the track. For the signal in ordinary state, it will not occur that a specific frequency component becomes always large. Therefore, to normally generate a pilot tone having an adequately large level, a special control is necessary after adding the redundant information for this purpose. Furthermore, if the redundant information to be added is too much, the recording density is high, and if accurate tracking be done, the reproduction error rate increases. In the invention, accordingly, by adding the redundant information only in the specific section in the track, it is intended to generate the pilot tone necessary for tracking only in this section. As a result, accurate tracking is possible without increasing the recording density so much.

Fig. 1(a) is an explanatory diagram of recording format of one track;

Fig. 1(b) is an explanatory diagram of minimum unit of one recording;

Fig. 2 is an explanatory diagram showing an example of track pattern on a magnetic tape;

Fig. 3 is an explanatory diagram of a constitution of parities of an error correction code in a first embodiment;

Fig. 4 is an explanatory diagram of bit division;

Fig. 5 is an explanatory diagram of a constitution of parities of an error correction code in a second embodiment; and

Fig. 6 is a block diagram of a circuit composition for realizing the invention.

A first embodiment of the invention is described below. As shown in Fig. 1(a), a track is composed of, sequentially from the beginning, a preamble 1, a first burst 2 composed of N_1 synchronous blocks, a gap 3, a second burst 4 composed of N_2 synchronous blocks, and a postamble 5. As shown in Fig. 1(b), a synchronous block which is the minimum unit of data processing in block recording is composed of a pattern 6 showing its beginning, an identification symbol 7 of the block, data 8, and parities of error correction code 9.

In such method of data error correction coding, for the data 10 (Fig. 3(a)) arranged two-dimensionally (rectangularly), first outer coding is effected in the row direction to add parities 11 of outer code (Fig. 3(b)), then inner coding is effected in the line direction to add parities 12a of inner code (Fig. 3 (c)). Next, rearranging the data in the line unit, the lines each consisting of the parities 11 of the outer code and the parities 12b of the inner code relating to these parities 11 are dispersed in between the lines each consisting of data 10a to 10d and parities 12c to 12f of the inner code relating to the data 10a to 10d (Fig. 3(d)). Here, supposing $K_1.k_1$ = $k_2.k_2$ (k_1, k_1, k_2, k_2 are natural values, and $k_1>k_2$), as shown in Fig. 4(a), data bit k1 having a space SP1 is divided again in every k_2 bits, and, as shown in Fig. 4(b), a space SP (k_1-k_2 pieces of 0) of every k_1-k_2 bits is inserted in every k_2 bits. This space SP is generated by raising the signal processing rate more than the blanking period of the video signal and the original data rate.

Consequently, parities 11a to 11c of outer codes of K_1 lines, and parities 12g to 12i of inner codes relating to the parities 11a to 11c are dispersed as patterns of K_2 lines. Afterwards, by adding the identifica-tion symbol 7, and modulating by using k_1/n conversion code for converting data word of k_1 bits into code word of n bits, the beginning pattern 6 is added to every inner code word, thereby composing the synchronous block. Meanwhile, this k_1/n conversion code is used for providing the bit stream to be recorded with a characteristic suited to the recording and reproducing system, and finally reducing the bit error rate. At this time, the parities of inner code corresponds to the parities 9. The modulation by k_1/n conversion code is actually considered to be modulated by the k_2/n modulation code in the portion 13 in which a space of every k_1-k_2 bits is inserted (shaded area in Fig. 3(e)). This is because the actual information quantity of the data word of k1 bits in which the space SP of k_1-k_2 bits is inserted, that is, the value taken by the data word, is only for k_2 bits.

Therefore, in the k_1/n conversion code, if not DC free, since $k_1>k_2$, it is possible to set DC free by the k_2/n conversion code. In this case, DC free state refers to the condition in which the DC components are few in the bit stream to be recorded, and the low frequency components near the DC are also few. The feature of such DC free state is that the individual difference of 1 and 0 in the bit stream to be recorded settles within a specific finite value regardless of the type of data. Naturally, for such feature, the code word to be recorded should be redundant, and the redundancy of the code word is higher in the k_2/n conversion code ($k_1>k_2$) than in the k_1/n conversion code, and the control of DC free state is easier. On the other hand, in the preamble 1, gap 3, and postamble 5, since the pattern can be set arbitrarily, the DC free pattern can be selected.

In such constitution, in this embodiment, the synchronous block composed of preamble 1, gap 3, postamble 5, and parity symbol of outer code may be set in DC free state. An example of pattern for setting the preamble 1, gap 3 and postamble 5 in DC free state is ...011001100110011001.... Supposing k_1=8, k_2=4, n=12, the DC free 4/12 conversion code is necessary, and an example is shown in Table 1. In this embodiment, meanwhile, it is enough as far as the frequency of the pilot tones of the tracks adjacent to the specific section is different, and the types of frequency of pilot tones may be enough with two.

Table 1

Data word	Code word	
(0000)	(1111 0011 0000)	= F30h
(0001)	(1110 0111 0000)	= E70h
(0010)	(1111 0001 1000)	= F18h
(0011)	(1110 0011 1000)	= E38h
(0100)	(1100 1111 0000)	= CF0h
(0101)	(1111 0000 1100)	= F0Ch
(0110)	(1100 0111 1000)	= C78h
(0111)	(1110 0001 1100)	= E1Ch
(1000)	(1100 1100 1100)	= CCCh
(1001)	(1100 0011 1100)	= C3Ch
(1010)	(1100 0000 1111)	= C0Fh
(1011)	(1111 0000 0111)	= F07h
(1100)	(1111 0000 0011)	= F03h
(1101)	(1100 0110 0011)	= C63h
(1110)	(1100 1100 0011)	= CC3h
(1111)	(1100 0011 0011)	= C33h

A second embodiment of the invention is described below. Different from the first embodiment, this embodiment is not intended to superpose the pilot tone analogously, but to generate digitally. Fig. 5 is an explanatory diagram of the composition of data and parities. In Fig. 5, numeral 12b is parity of inner code. The composition of the track and synchronous block is same as in the first embodiment. The data error correction coding method shown in Fig. 5 is to first apply outer coding in the row direction to the data 10 arranged two-dimensionally (rectangularly) (Fig. 5 (a)), and parities 11 of outer code are added (Fig. 5(b)). Rearranging the data in the line unit, the lines 11a to 11c composed of parities of outer code are dispersed among lines 10a to 10d composed of data (Fig. 5 (d)). Here, same as in the first embodiment, supposing $K_1.k_1=K_2.k_2$ (K_1, k_1, K_1, k_2 being natural numbers, and $kr_1>k_2$), and, as shown in Fig. 2, the data k1 bits having a space SP1 are divided again into every k_2 bits, and the space SP (k_1-k_2 pieces of 0) of every k_1-k_2 bits is inserted in every k_2 bits. This space is generated by raising the signal processing rate higher than the blanking period of video signal, and the original data rate.

Therefore, the parities 11a to 11c of outer codes of K1 lines are dispersed as patterns of K_2 lines. Afterwards, after adding the parities 12b of the inner code by inner coding in the line direction, the identification symbol 7 is added, and modulation is effected by using k1/n conversion code. Furthermore, by adding the beginning pattern 6 to every inner word, a synchronous block is composed. At this time, the parities 12b of the inner code corresponds to the parities 9. Same as in the first embodiment, in the parts 14a to 14c (shaded area in Fig. 5(e)) where a space of every k_1-k_2 bits is inserted, modulation by k2/n conversion code is effected, so that the DC may be set free.

In such constitution, in this embodiment, the synchronous block composed of preamble 1, gap 3, postamble 5, and inspection symbol of outer code may be set in DC free state. An example of pattern for setting DC free in the synchronous block composed of preamble 1, gap 3, postamble 5 and parities of outer code, and an example of conversion code for setting DC free in the synchronous block composed of parities of outer code may be same as in the first embodiment.

A third embodiment of the invention is described below. In the portion where DC can be set free in the first embodiment (the parts 13a to 13c in which the preamble 1, gap 3, postamble 5, and space of every k_1-k_2 bits are inserted, (or the shaded area in Fig. 3 (e)), the pilot tone can be inserted digitally. First, an example of pattern for setting DC free the preamble 1, gap 3, and postamble 5 is shown below. Supposing n=12, two types of 12-bit pattern are considered, that is, C1=(1111 0011 1100), C2=(0000 1100 0011); using the pattern repeating C1, C2 three times each,

..., C_2, C_1, C_1, C_1, C_2, C_2, C_2, C_1, C_1, C_1, C_2, C_2, C_2, C_1, C_1, C_1, C_2, C_2, C_2, C_1, ...

and the pattern repeating C_1, C_2 six times each,

..., C_2, C_1, C_1, C_1, C_1, C_1, C_1, C_2, C_2, C_2, C_2, C_2, C_2, C_1, C_1, C_1, C_1, C_1, C_1, C_2, ...

pilot tones of two types of frequency can be generated. In all of preamble, gap and postamble, it is advantageous because the recording rate is not increased even when digitally generating pilot tones.

Furthermore, by the modulation with the k_2/n conversion code used in the space inserted portion, it is possible to generate pilot tones. An example of 4/12 conversion code necessary when supposing k_1=8, k_2=4, n=12 is given in Table 2. Actually, the code words in Table 2 are in pair with the inverted code words obtained by inverting 0 to 1, and 1 to 0, and pilot tones of two different frequencies can be generated by using the pattern obtained by repeating the code word and inverted code word three times each, and the pattern obtained by

repeating the code word and inverted code word six times each.

Table 2

Data word	Code word
(0000)	(0011 1110 0111) = 3E7
(0001)	(0011 1100 1111) = 3CF
(0010)	(1111 1001 1100) = F9C
(0011)	(1110 0011 1100) = E3C
(0100)	(1110 0111 1100) = E7C
(0101)	(1100 1111 1100) = CFC
(0110)	(0011 1111 0011) = 3F3
(0111)	(1111 0000 1111) = F0F
(1000)	(1111 1000 0111) = F87
(1001)	(1100 1100 1111) = CCF
(1010)	(1110 0110 0111) = E67
(1011)	(1100 1110 0111) = CE7
(1100)	(1110 0111 0011) = E73
(1101)	(1100 1111 0011) = CF3
(1110)	(1111 0011 0011) = F33
(1111)	(0011 1111 1100) = 3FC

Having such constitution, in this embodiment, a pilot tone can be generated from the synchronous block composed of the preamble 1, gap 3, postamble 5, and parities of outer code. In this embodiment, meanwhile, two patterns are used for preamble and others, and the number of repetitions of code word and inverted code word of 4/12 conversion code is taken as three times and six times, but these are not limitative. Also a pattern capable of generating pilot tones of two or more different frequencies is also possible.

In the invention, meanwhile, as the error correction code, a method of composing DC free block and a method of generating a digital pilot, by using sum codes possessing Inner code and outer code are explained, but a similar constitution is also possible for other error correcting code. Or, instead of DC free control or pilot tone generation control by using all of parities of outer codes, only a part of the parities may be used. Furthermore, instead of composing one synchronous block from one inner code word, it is also possible to compose of a plurality of inner code words. The number of data bursts provided in one track is not limited to two, but may be other arbitrary number. The preamble length, gap length, and postamble length may not necessarily be integer multiples of the synchronous block length. These patterns of the embodiments are only examples, and it is not necessary to limit to the values of k_1=8, k_2=4, n=12. In the embodiment, it is enough as far as the frequencies of the pilot tones of the tracks adjacent to a specific section are different, and the types of the frequency of pilot tones may be enough with two.

Finally, means for realizing the first embodiment of the invention is explained by referring to Fig. 6. In Fig. 6, the data 10 arranged two-dimensionally (rectangularly) as shown in Fig. 3(a) by the known art is sent into an outer error encoder 15 sequentially In the row direction, and parities 11 of outer code is added as shown in Fig. 3(b), and is stored in a memory circuit 16. The data stored in the memory circuit 16 in the row direction is read out in the line direction, and the data is provided with the parities 12a of the inner code in an inner error encoder, as shown in Fig. 3(c), and is delivered. The data is stored in a memory circuit 18 sequentially in the line direction. From the memory circuit 18, the data is read out in the line direction in the sequence as shown in Fig. 3(d). Such reading control is effected in a reading control circuit 19. The reading control circuit 19 generates the reading address in the line direction of the memory in the memory circuit 18 so that the output may be obtained as shown in Fig. 3(d), which involves no technical difficulty. The output of the memory circuit 18 is recorded in a magnetic tape 22 through a recording circuit 20 composed of amplifier and others, and a recording head 21.

On the other hand, when reproducing, the reproduction signal from the magnetic tape 22 is stored in a memory circuit 25 through a magnetic head 23, and a reproduction circuit 24 composed of reproduction amplifier and others. The output of the reproduction circuit 24 is in the form of Fig. 3(d), and a write control circuit 26 stores the output of the reproduction circuit 24 in the memory circuit 26 in a form of Fig. 3(c). This operation is the reverse operation of the read control circuit 19, and the write address in the line direction into the memory in the memory circuit 26 is generated. The output from the memory circuit 26 corrects the error in the line direction in an inner error decoder 27, that is, the error in the data in the synchronous block shown in Fig. 1(b) is corrected by using the parities, thereby removing the beginning pattern, identification symbols and parities, and the data is stored in a memory circuit 28 in the form of Fig. 3(b). The output of the memory circuit 28 is read in

the row direction, and the error in the row direction is corrected by using the parities of outer code in an outer error decoder 29, and the data is delivered in the form being rid of these parities. As a result, the data is in the two-dimensional (rectangular) form of Fig. 3(a), so that the original data is completely restored.

In Fig. 6, it is explained on the basis that the memory circuits 16, 28 and 19, 26, and the heads 21, 23 are independently provided, but where it is not necessary to record and reproduce simultaneously, these memory circuits and heads can be shared, and the circuit can be reduced. Fig. 6 is presented as means for realizing the first embodiment of the invention, but it is evident that the second and third embodiments can be realized by similar circuits. Thus, the invention realizes tracking of high precision in a very simple circuit constitution, and achieves to lower the error rate.

Claims

1. A method of a digital signal recording for superposing and recording pilot tones in tracks formed on a recording medium, and tracking by using crosstalk of the pilot tones when reproducing, wherein only a specific section in a track is set in DC free state, the pilot tones are not superposed in this section, and tracking is performed on the basis of the crosstalk of the pilot tones from adjacent tracks in the specific section when reproducing.

2. A method of claim 1, wherein the specific section is all or a part of a preamble section provided at a sarting end of the track.

3. A method of claim 1, wherein the specific section is all or a part of a postamble section provided at a terminal end of the track.

4. A method of claim 1, wherein the track possesses a plurality of data bursts composed of a plurality of synchronous blocks, and the specific section is all or a part of a gap section provided between the data bursts.

5. A method of claim 1, wherein data corresponding to the specific section is all or a part of parities of error correction.

6. A method of claim 5, wherein DC free control is effected on all data excluding a beginning pattern and identification symbol in a synchronous block corresponding to the specific section.

7. A method of claim 5, wherein DC free control is effected on all data excluding a beginning pattern, identification symbol, and parities of error correction added to each synchronous code in a synchronous block corresponding to the specific section.

8. A method of claim 6 or 7, wherein 4/12 conversion code is used for a signal in a portion for DC free control, and 8/12 conversion code is used for a signal in a portion not applying for DC free control.

9. A method of controlling a signal to be recorded so that a pilot tone may be generated in a specific section in a track formed on a recording medium, and tracking on the basis of a crosstalk of the pilot tone from a track adjacent to the specific section when reproducing.

10. A method of claim 9, wherein the specific section is all or a part of a preamble section provided at a starting end of the track.

11. A method of claim 9, wherein the specific section is all or a part of a postamble section provided at a final end of the track.

12. A method of claim 9, wherein the track possesses data bursts composed of a plurality of synchronous blocks, and the specific section is all or a part of a gap section provided between the data bursts.

13. A method of claim 9, wherein the track possesses data bursts composed of a plurality of synchronous blocks, and data corresponding to the specific section is a parity of error correction.

14. A method of claim 13, wherein pilot tone generation control is not effected on a beginning pattern and identification symbol in a synchronous block corresponding to the specific section.

15. A method of claim 13, wherein pilot tone control is not effected on a beginning pattern, identification symbol and parity of error correction added to each synchronous code in a synchronous block corresponding to the specific section.

16. A method of claim 14 or 15, wherein 4/12 conversion code is used for a signal in a portion for pilot tone generation control, and 8/12 conversion code is used for a signal in a portion not applying for pilot tone generation control.

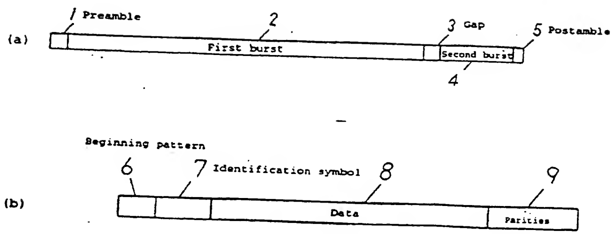
(a)
1 Preamble
2
First burst
3 Gap
Second burst
4
5 Postamble
(b)
Beginning pattern
6
7 Identification symbol
8
Data
9
Parities

Fig. 1

(a)

(b)

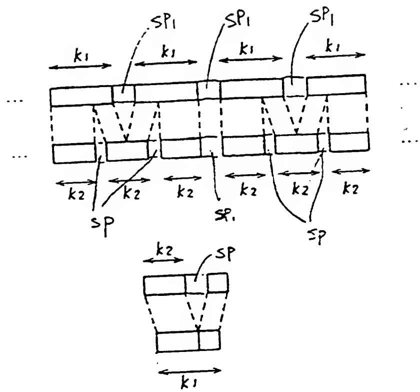

Fig. 4

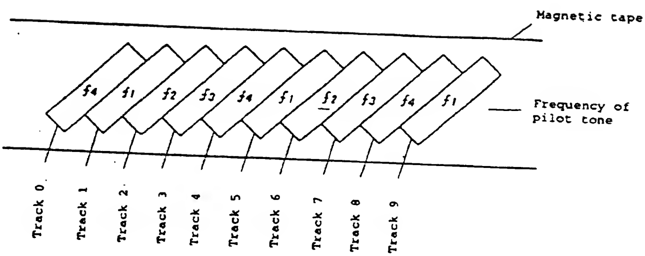
Magnetic tape
f4
f1
f2
f3
f4
f1
f2
f3
f4
f1
Frequency of pilot tone
Track 0
Track 1
Track 2
Track 3
Track 4
Track 5
Track 6
Track 7
Track 8
Track 9

Fig. 2

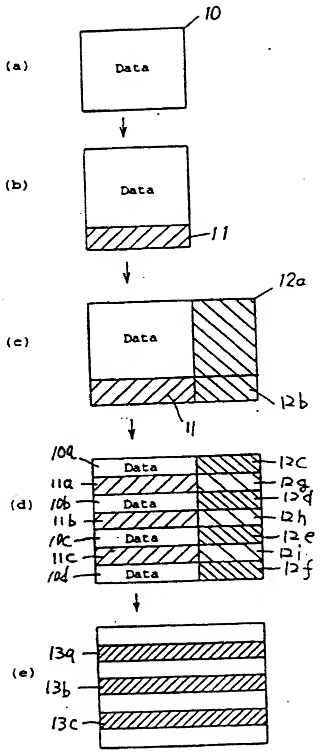
10
(a)
Data
(b)
Data
11
12a
(c)
Data
12b
11
10a
Data
12c
11a
12g
10b
Data
12d
(d)
11b
12h
10c
Data
12e
11c
12i
10d
Data
12f
13a
(e)
13b
13c

Fig. 3

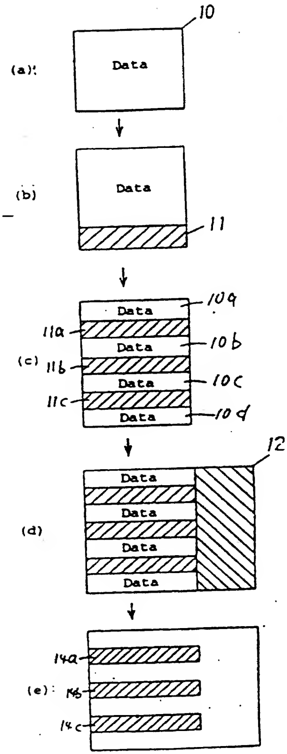
10
(a)
Data
(b)
Data
11
10a
Data
11a
Data
10b
(c)
11b
Data
10c
11c
Data
10d
12
Data
Data
(d)
Data
Data
14a
(e)
14b
14c

Fig. 5

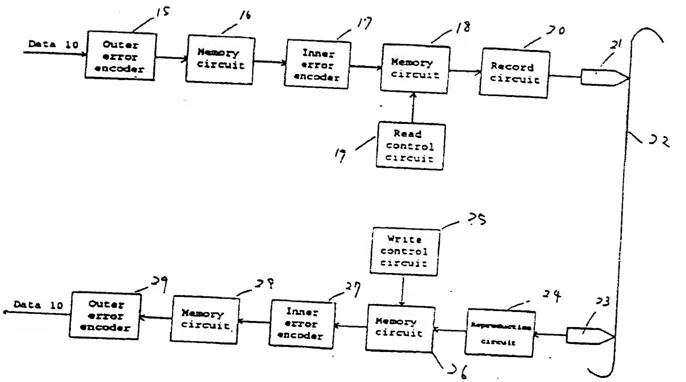
Data 10
Outer error encoder
Memory circuit
Inner error encoder
Memory circuit
Record circuit
Read control circuit
Write control circuit
Data 10
Outer error encoder
Memory circuit
Inner error encoder
Memory circuit
Reproduction circuit
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29

Fig. 6

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 91307181.7

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	US - A - 4 943 873 (KAWASAKI) * Abstract; fig. 4,5; column 1, lines 41-60; column 5, line 66 - column 6, line 15 * --	1-7, 9-15	G 11 B 5/584 G 11 B 20/10
X	US - A - 4 839 755 (YAMADA) * Fig. 1,2,16,24-27; claims * --	1,9	
X	US - A - 4 755 893 (YAMADA) * Abstract; fig. 1A,1B,3; claims 1,29 * --	1,9	
X	EP - A1 - 0 339 724 (PHILIPS) * Fig. 8; page 7, lines 41-53; claims 1,7 * --	1,9	
A	EP - A2 - 0 348 132 (SONY) * Fig. 1,11,14,15; column 9, lines 50-52; column 10, lines 36-42 * ----	8,16	TECHNICAL FIELDS SEARCHED (Int. Cl.5) G 11 B 5/00 G 11 B 20/00 G 11 B 21/00 H 04 N 5/00

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	09-10-1991	DIMITROW

CATEGORY OF CITED DOCUMENTS

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